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The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) A memory array comprising:
a plurality of two-terminal memory plugs, each two-terminal memory plug operable to change from a high resistive state to a low resistive state upon application of a first write voltage and change from a low resistive state to a high resistive state upon application of a second write voltage, and each two terminal memory plug including a multi-resistive state element that includes a conductive element and a reactive metal that reacts with the conductive element.
2. (Original) The memory array of claim 1, wherein the reactive metal has fully reacted with the conductive element.
3. (Original) The memory array of claim 1, wherein each two-terminal memory plug includes a bottom electrode at one of the terminals and a top electrode at the other terminal.
4. (Original) The memory array of claim 3, wherein:
the bottom electrode is deposited before the conductive element;
the reactive metal is deposited on the conductive element after deposition of the conductive element; and
the top electrode is deposited after the deposition of the reactive metal.

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5. (Original) The memory array of claim 4, wherein no portion of the reactive metal between the conductive element and the top electrode is unreacted with the conductive element.
6. (Original) The memory array of claim 4, wherein an anneal step is used after deposition of the reactive metal and prior to deposition of the top electrode.
7. (Original) The memory array of claim 4, wherein an anneal step is used after deposition of both the reactive metal and the top memory electrode.
8. (Original) The memory array of claim 1, wherein each two-terminal memory plug can be exposed to a range of voltages without disturbing the resistive state of the memory plug.
9. (Original) The memory array of claim 1, wherein the multi-resistive state element is substantially non-conductive over a range of voltages from V_{NO-} to V_{NO+} .
10. (Original) The memory array of claim 9, wherein a manganite perovskite is used as the conductive element.
11. (Original) The memory array of claim 10, wherein the manganite perovskite is a PCMO.
12. (Original) The memory array of claim 11, wherein a reactive metal that can react with the PCMO is Al, Ti, Mg, W, Fe, Cr, Vn, Zn, Ta or Mo.

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13. (Original) The memory array of claim 12, wherein the reactive metal is Al.
14. (Original) The memory array of claim 12, wherein 10 - 100 Angstroms of Al is deposited on the PCMO.
15. (Original) The memory array of claim 14, wherein 25 - 50 Angstroms of Al is deposited on the PCMO.
- 16 - 26. (Cancelled)